

Fig. 2

- a)
10 Image processing IC
21 Camera
22 Camera I/F circuit
23 Buffer memory
24 Transfer address generating circuit
25 Area memory
26 Address converting circuit
26A Buffer memory control circuit
27 Area register control circuit
40 Work memory
60 Display panel

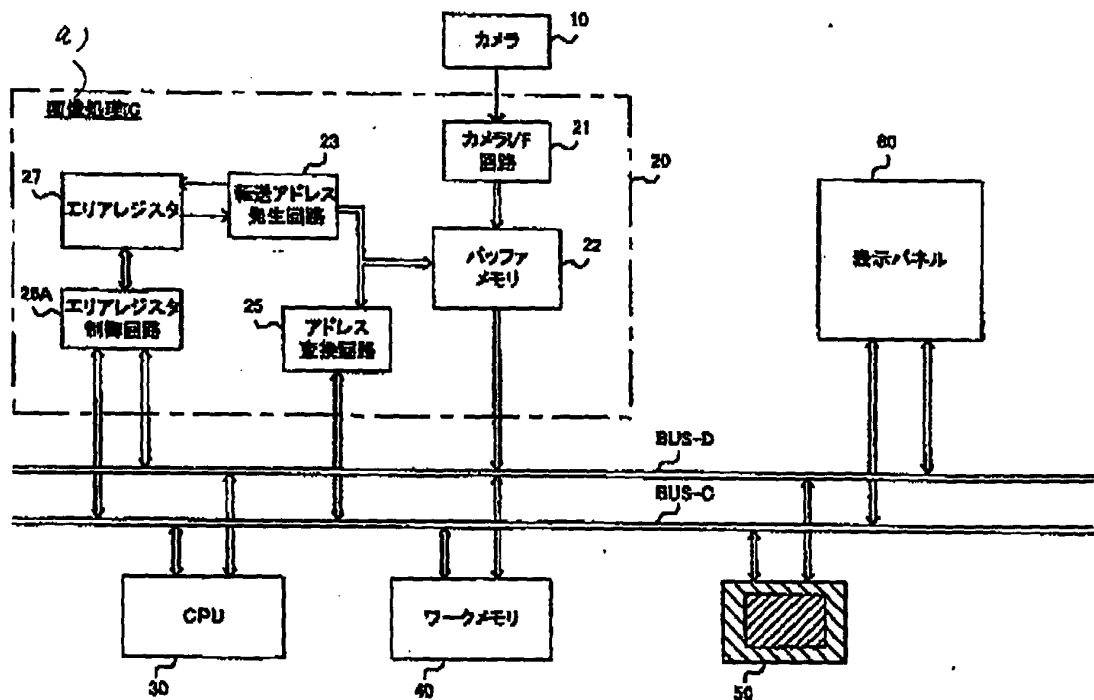


Fig. 3

- a) Image processing IC
10 Camera
21 Camera I/F circuit
22 Buffer memory
23 Transfer address generating circuit
24 Area memory
25 Address converting circuit
26 Buffer memory control circuit
28 Read-out address generating circuit
29 Gate circuit
40 Work memory
60 Display panel

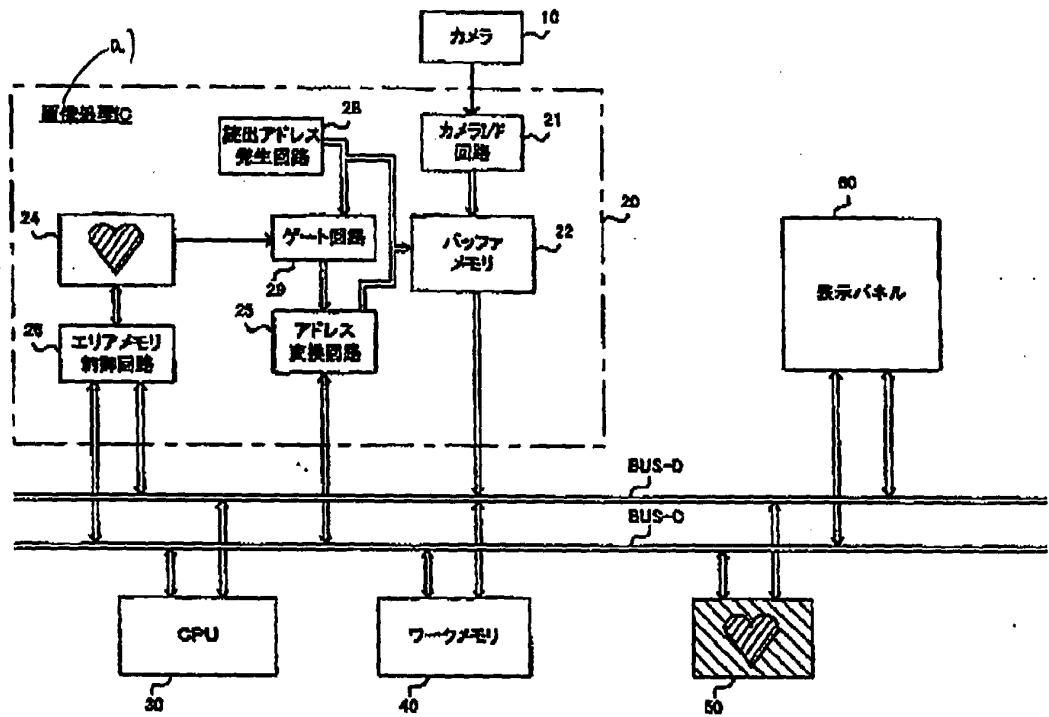


Fig. 4

- a) Image processing IC
10 Camera
21 Camera I/F circuit
22 Buffer memory
23 Transfer address generating circuit
24 Area memory
25 Address converting circuit
26 Buffer memory control circuit
26B Read-out address generating circuit
28 Gate circuit
29 Work memory
40 Display panel

